Form PTO-1449 (modified)	Atty. Docket No.: 102-0069US-1	Serial No.: ~~UNKNOWN~~ 10/706,003
List of Patents and Publications for Applicant's INFORMATION DISCLOSURE STATEMENT	Applicant: Ronnie M. Harrison	Title: A Delay Lock Loop Circuit Useful In A Synchronous System And Associated Methods
(Use several sheets if necessary)	Filing Date: ~~herewith~~ 11/12/03	Group: ~~UNKNOWN~~ 2818

U.S. Patent Documents	Foreign Patent Documents	Other Art
See Page 1	*See Page 1*	*See Page 1-4*

U.S. Patent Documents

Exam. Init.	Ref. Des	Document Number	Date	Name	Class	Sub Class	Filing Date of App.
	A1	6,424,178	July 23, 2002	Harrison	326	93	Aug. 30, 2000
	A2	6,173,432	Jan. 9, 2001	Harrison	716	1	June 20, 1997
	A3	6,069,506	May 30, 2000	Miller et al.	327	156	May 20, 1998
	A4	6,011,732	Jan. 4, 2000	Harrison et al.	365	194	Aug. 20, 1997
	A5	5,940,609	Aug. 17, 1999	Harrison	395	558	Aug. 29, 1997
	A6	5,926,047	July 20, 1999	Harrison	327	159	Aug. 29, 1997
	A7	5,920,518	July 6, 1999	Harrison et al.	365	233	Feb. 11, 1997
	A8	4,902,986	Feb. 20, 1990	Lesmeister	331	25	Jan. 30, 1989
	A9	2001/0015664	Aug. 23, 2001	Taniguchi	327	158	Feb. 7, 2001
	A10	2002/0180500	Dec. 5, 2002	Okuda et al.	327	158	July 25, 2002
	A11	6,215,725	Apr. 10, 2001	Komatsu	365	233	July 21, 1998
	A12	6,316,976	Nov. 13, 2001	Miller Jr. et al.	327	156	Apr. 28, 2000

Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1	X					
	B2	X					

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Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
	C1	U.S. Patent Application Filed June 28, 2001, Serial No. 09/896,030, Titled "Method And System For Adjusting The Timing Offset Between A Clock Signal And Respective Digital Signals Transmitted Along With That Clock Signal, And Memory Device And Computer System Using Same," Inventor – Harrison et al., pp. 1-55, 7 drawing sheets.
	C2	U.S. Patent Application Filed March 1, 1999, Serial No. 09/260,212, Titled "Method And Apparatus For Generating A Phase Dependent Control Signal," Inventor – Harrison, pp. 1-34, 7 drawing sheets.
	C3	U.S. Patent Application Filed February 26, 1999, Serial No. 09/259,625, Titled "Interlaced Delay-Locked Loops For Controlling Memory-Circuit Timing," Inventor - Harrison, pp. 1-29, 11 drawing sheets.
	C4	Descriptive literature entitled, "400 MHz SLDRAM, 4Mx16 SLDRAM Pipelined, Eight Bank, 2.5 V Operation," pp. 1-22.
	C5	"Draft Standard for a High-Speed Memory Interface (SyncLink)," Microprocessor and Microcomputer Standards Subcommittee of the IEEE Computer Society, Copyright 1996 by the Institute of Electrical and Electronics Engineers, Inc., New York, NY, pp. 1-56.
	C6	Lesmeister, Gary, "A Densely Integrated High Performance CMOS Tester," International Test Conference 1991, Paper 16.2, pp. 426-429.
	C7	Chapman et al., "A Low-Cost High-Performance CMOS Timing Vernier for ATE," International Test Conference, Copyright 1995 IEEE, Paper 21.2, pp. 459-468.
	C8	Novof et al., "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and ±50 ps Jitter," Nov. 1995, IEEE Journal of Solid-State Circuits, vol. 30, no. 11, pp. 1259-1266.
	C9	Christiansen, Jorgen , "An Integrated High Resolution CMOS Timing Generator Based on an Array of Delay Locked Loops," July 1996, IEEE Journal of Solid-State Circuits, vol. 31, no. 7, pp. 952-957.
	C10	Combes et al., "A Portable Clock Multiplier Generator Using Digital CMOS Standard Cells," July 1996, IEEE Journal of Solid-State Circuits, vol. 31, no. 7, pp. 958-965.

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Exam. Init.	Ref. Des.	Citation
	C11	Yoshimura et al., "A 622-Mb/s Bit/Frame Synchronizer for High-Speed Backplane Data Communication," July 1996, IEEE Journal of Solid-State Circuits, vol. 31, no. 7, pp. 1063-1066.
	C12	Saeki et al., "A 2.5-ns Clock Access, 250-MHz, 256-Mb SDRAM with Synchronous Mirror Delay," Nov. 1996, IEEE Journal of Solid-State Circuits, vol. 31, no. 11, pp. 1656-1665.
	C13	Kaenel et al., "A 320 MHz, 1.5mW @ 1.35 V CMOS PLL for Microprocessor Clock Generation," Nov. 1996, IEEE Journal of Solid-State Circuits, vol. 31, no. 11, pp. 1715-1722.
	C14	Maneatis, John G., "Low-Jitter Process-Independent DLL and PLL Based of Self-Biased Techniques," Nov. 1996, IEEE Journal of Solid-State Circuits, vol. 31, no. 11, pp. 1723-1732.
	C15	Donnelly et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 μm – 0.7 μm CMOS ASIC," Dec. 1996, IEEE Journal of Solid-State Circuits, vol. 31, no.12, pp.1995-2001.
	C16	Sidiropoulos et al., "A Semidigital Dual Delay-Locked Loop," Nov. 1997, IEEE Journal of Solid-State Circuits, vol. 32, no. 11, pp. 1683-1692.
	C17	Goto et al., "A PLL-Based Programmable Clock Generator with 50 to 350 MHz Oscillating Range for Video Signal Processors," IEICE Trans. Electron., Dec. 1994, vol. E77-C, no. 12, pp. 1951-1956.
	C18	Alvarez et al., "A Wide-Bandwidth Low-Voltage PLL for PowerPC™ Microprocessors," IEICE Trans. Electron., June 1995, vol. E78-C, no. 6, pp. 631-639.
	C19	Tanoi et al., "A 250-622 Mhz Deskew and Jitter-Suppressed Clock Buffer Using Two-Loop Architecture," IEICE Trans. Electron., July 1996, vol. E79-C, no. 7, pp. 898-904.
	C20	Sidiropoulos et al., "A CMOS 500 Mbps/pin Synchronous Point to Point Link Interface," 1994 Symposium on VLSI Circuits Digest of Technical Papers, No. 4.5, pp. 43-44.
	C21	Soyuer et al., "A Fully Monolithic 1.25GHz CMOS Frequency Synthesizer," 1994 Symposium on VLSI Circuits Digest of Technical Papers, No. 11.3, pp. 127-128.
	C22	Tanoi et al., "A 250-622 Mhz Deskew and Jitter-Suppressed Clock Buffer Using a Frequency- and Delay-Locked Two-Loop Architecture," 1995 Symposium on VLSI Circuits Digest of Technical Papers, No. 11-2, pp. 85-86.

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Exam. Init.	Ref. Des.	Citation
	C23	Nakamura et al., "A 156 Mbps CMOS Clock Recovery Circuit for Burst-mode Transmission," 1996 Symposium on VLSI Circuits Digest of Technical Papers, No. 11.4, pp. 122-123.
	C24	Portmann et al., "A Multiple Vendor 2.5-V DLL for 1.6-GB/s RDRAMs," 1999 Symposium on VLSI Circuits Digest of Technical Papers, No. 15-3, pp. 153-156.
	C25	Ishibashi et al., "A High-Speed Clock Distribution Architecture Employing PLL for 0.6μm CMOS SOG," IEEE 1992 Custom Integrated Circuits Conference, pp. 27.6.1-27.6.4.
	C26	Ko et al., "A 30-ps Jitter, 3.6-μs Locking, 3.3-Volt Digital PLL for CMOS Gate Arrays," IEEE 1993 Custom Integrated Circuits Conference, pp. 23.3.1-23.3.4.
	C27	Kim et al., "A 30MHz High-Speed Analog/Digital PLL in 2μm CMOS," 1990 IEEE International Solid-State Circuits Conference, Session 6: High-Speed Analog, TAM 6.4, pp.105-105.
	C28	Lee et al., "A 2.5 V Delay-Locked Loop for an 18Mb 500MB/s DRAM," 1994 IEEE International Solid-State Circuits Conference, Session 18: High-Performance Logic and Circuit Techniques, Paper FA 18.6, pp.300-301.
	C29	Ljuslin et al., "An Integrated 16-channel CMOS Time to Digital Converter," 1993 IEEE Conference Record: Nuclear Science Symposium & Medical Imaging Conference Vol. 1, pp. 625-629.
	C30	Shirotori et al., "PLL-based, Impedance Controlled Output Buffer," Toshiba Microelectronics Corp., pp. 49-50.
	C31	

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